In the Specification:

Please amend para [0031] as follows:

[0031] The trench DMOS transistor is completed by forming and patterning a BPSG layer **46** over the structure to define BPSG regions associated with the gate electrodes. The BPSG are patterned through a contact mask and etching process to extend over the top of the trench, after which successive layers of Ti/TiN **48** and AL/Si/Cu **50** are deposited through a metal mask and etching process. Also, a drain contact layer **49** is formed on the bottom surface of the substrate. Finally, a pad mask is used to define pad contacts.